19-4185; Rev 0; 8/08

Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

General Description

The MAX19985A high-linearity, dual-channel, downconversion mixer is designed to provide approximately 8.7dB gain, +25.5dBm of IIP3, and 9.0dB of noise figure for 700MHz to 1000MHz diversity receiver applications. With an optimized LO frequency range of 900MHz to 1300MHz, this mixer is ideal for high-side LO injection architectures in the cellular and new 700MHz bands. Low-side LO injection is supported by the MAX19985, which is pin-pin and functionally compatible with the MAX19985A.

In addition to offering excellent linearity and noise performance, the MAX19985A also yields a high level of component integration. This device includes two double-balanced passive mixer cores, two LO buffers, a dual-input LO selectable switch, and a pair of differential IF output amplifiers. On-chip baluns are also integrated to allow for single-ended RF and LO inputs.

The MAX19985A requires a nominal LO drive of 0dBm and a typical supply current of 330mA at V_{CC} = +5.0V or 280mA at V_{CC} = +3.3V.

The MAX19985/MAX19985A are pin compatible with the MAX19995/MAX19995A series of 1700MHz to 2200MHz mixers and pin similar with the MAX19997A/MAX19999 series of 1850MHz to 3800MHz mixers, making this entire family of downconverters ideal for applications where a common PCB layout is used across multiple frequency bands.

The MAX19985A is available in a 6mm x 6mm, 36-pin thin QFN package with an exposed pad. Electrical performance is guaranteed over the extended temperature range of T_C = -40°C to +85°C.

Applications

850MHz WCDMA and cdma2000® Base Stations

700MHz LTE/WiMAX™ Base Stations

GSM850/900 2G and 2.5G EDGE Base Stations

iDEN® Base Stations

Fixed Broadband Wireless Access

Wireless Local Loop

Private Mobile Radios

Military Systems

Features

- **700MHz to 1000MHz RF Frequency Range**
- **900MHz to 1300MHz LO Frequency Range**
- **50MHz to 500MHz IF Frequency Range**
- **8.7dB Typical Conversion Gain**
- **9.0dB Typical Noise Figure**
- **+25.5dBm Typical Input IP3**
- **+12.6dBm Typical Input 1dB Compression Point**
- **76dBc Typical 2LO-2RF Spurious Rejection at P_{RF} = -10dBm**
- **Dual Channels Ideal for Diversity Receiver Applications**
- **48dB Typical Channel-to-Channel Isolation**
- **Low -3dBm to +3dBm LO Drive**
- **Integrated LO Buffer**
- **Internal RF and LO Baluns for Single-Ended Inputs**
- **Built-In SPDT LO Switch with 46dB LO1-to-LO2 Isolation and 50ns Switching Time**
- **Pin Compatible with the MAX19995/MAX19995A Series of 1700MHz to 2200MHz Mixers**
- **Pin Similar to the MAX19997A/MAX19999 Series of 1850MHz to 3800MHz Mixers**
- **Single +5.0V or +3.3V Supply**
- **External Current-Setting Resistors Provide Option for Operating Device in Reduced-Power/Reduced-Performance Mode**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX19985AETX+	-40°C to +85°C	36 Thin QFN-EP*
MAX19985AETX+T	-40°C to +85°C	36 Thin QFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

cdma2000 is a registered trademark of Telecommunications Industry Association.

WiMAX is a trademark of WiMAX Forum.

iDEN is a registered trademark of Motorola, Inc.

Typical Application Circuit and Pin Configuration appear at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +5.5V
LO1, LO2 to GND ....±0.3V
Any Other Pins to GND...............................-0.3V to (V_{CC} + 0.3V)
RFMAIN, RFDIV, and LO_ Input Power ....+15dBm
RFMAIN, RFDIV Current (RF is DC shorted to GND through balun)...50mA
Continuous Power Dissipation (Note 1) 8.8W
θ_{JA} (Notes 2, 3)..+38°C/W
θ_{JC} (Note 3)...7.4°C/W
Operating Temperature Range (Note 4).....T_C = -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.
Note 2: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.
Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.
Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+5.0V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5.0V, T_C = +25°C, all parameters are production tested, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}			330	380	mA
LOSEL Input High Voltage	V_{IH}		2			V
LOSEL Input Low Voltage	V_{IL}				0.8	V
LOSEL Input Current	I_{IH}, I_{IL}		-10		+10	µA

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = 3.0V to 3.6V, T_C = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, T_C = +25°C, all parameters are guaranteed by design and not production tested, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	R2 = R5 = 600Ω	3.0	3.3	3.6	V
Supply Current	I_{CC}	Total supply current, V_{CC} = 3.3V		280		mA
LOSEL Input High Voltage	V_{IH}			2		V
LOSEL Input Low Voltage	V_{IL}			0.8		V

RECOMMENDED AC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 5)	700		1000	MHz
LO Frequency	f_{LO}	(Note 5)	900		1300	MHz
IF Frequency	f_{IF}	Using Mini-Circuits TC4-1W-17 4:1 transformer as defined in the *Typical Application Circuit*, IF matching components affect the IF frequency range (Note 5)	100		500	MHz
		Using alternative Mini-Circuits TC4-1W-7A 4:1 transformer, IF matching components affect the IF frequency range (Note 5)	50		250	
LO Drive Level	P_{LO}	(Note 5)	-3		+3	dBm

+5.0V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = +4.75V to +5.25V, RF and LO ports are driven from 50Ω sources, P_{LO} = -3dBm to +3dBm, P_{RF} = -5dBm, f_{RF} = 700MHz to 1000MHz, f_{LO} = 900MHz to 1200MHz, f_{IF} = 200MHz, $f_{RF} < f_{LO}$, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} =900MHz, f_{LO} = 1100MHz, f_{IF} = 200MHz, T_C =+25°C, all parameters are guaranteed by design and characterization, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Power Gain	G_C	f_{IF} = 200MHz, f_{RF} = 824MHz to 915MHz, T_C = -40°C to +85°C	7.0	8.7	10.2	dB
		f_{IF} = 200MHz, f_{RF} = 824MHz to 915MHz, T_C = +25°C (Note 9)	7.7	8.7	9.7	
Conversion Power Gain Variation vs. Frequency	ΔG_C	Flatness over any one of three frequency bands: f_{RF} = 824MHz to 849MHz, f_{RF} = 869MHz to 894MHz, f_{RF} = 880MHz to 915MHz (Note 9)		0.15	0.3	dB
Gain Variation Over Temperature	TC_G	T_C = -40°C to +85°C		-0.012		dB/°C
Noise Figure	NF	T_C = -40°C to +85°C		9.2	11.5	dB
		f_{RF} = 850MHz, f_{IF} = 200MHz, P_{LO} = 0dBm, T_C = +25°C, V_{CC} = +5.0V		9.0	10.3	
Noise Figure Temperature Coefficient	TC_{NF}	T_C = -40°C to +85°C		0.018		dB/°C
Noise Figure Under Blocking Condition	N_{FB}	+8dBm blocker tone applied to RF port, f_{RF} = 900MHz, f_{LO} = 1090MHz, P_{LO} = -3dBm, $f_{BLOCKER}$ = 800MHz, V_{CC} = +5.0V (Note 7)		18.8	22	dB
Input 1dB Compression Point	IP_{1dB}	T_C = -40°C to +85°C	10.0	12.6		dBm
		T_C = +25°C (Note 9)	11.0	12.6		
Third-Order Input Intercept Point	IIP3	f_{RF} = 824MHz to 915MHz, f_{RF1} - f_{RF2} = 1MHz, f_{IF} = 200MHz, P_{RF} = -5dBm/tone, T_C = -40°C to +85°C	22.5	25.5		dBm
		f_{RF} = 824MHz to 915MHz, f_{RF1} - f_{RF2} = 1MHz, f_{IF} = 200MHz, P_{RF} = -5dBm/tone, T_C = +25°C (Note 9)	23.5	25.5		

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+5.0V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = +4.75V to +5.25V, RF and LO ports are driven from 50Ω sources, P_{LO} = -3dBm to +3dBm, P_{RF} = -5dBm, f_{RF} = 700MHz to 1000MHz, f_{LO} = 900MHz to 1200MHz, f_{IF} = 200MHz, $f_{RF} < f_{LO}$, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} =900MHz, f_{LO} = 1100MHz, f_{IF} = 200MHz, T_C =+25°C, all parameters are guaranteed by design and characterization, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
2LO-2RF Spur Rejection	2 x 2	f_{RF} = 800MHz, f_{LO} = 1000MHz, f_{SPUR} = 900MHz	P_{RF} = -10dBm	-63	-76		dBc
			P_{RF} = -5dBm (Note 9)	-58	-71		
3LO-3RF Spur Rejection	3 x 3	f_{RF} = 800MHz, f_{LO} = 1000MHz, f_{SPUR} = 933.3MHz	P_{RF} = -10dBm	-65	-78		dBc
			P_{RF} = -5dBm (Note 9)	-60	-73		
LO Leakage at RF Port		f_{LO} = 900MHz to 1300MHz, P_{LO} = +3dBm (Note 10)			-40	-20	dBm
2LO Leakage at RF Port		f_{LO} = 900MHz to 1200MHz, P_{LO} = +3dBm (Note 10)			-38	-25	dBm
		f_{LO} = 1200MHz to 1300MHz, P_{LO} = +3dBm (Note 10)			-35	-22	
3LO Leakage at RF Port		f_{LO} = 900MHz to 1300MHz, P_{LO} = +3dBm (Note 10)			-50	-28	dBm
4LO Leakage at RF Port		f_{LO} = 900MHz to 1300MHz, P_{LO} = +3dBm (Note 9)			-25	-15	dBm
LO Leakage at IF Port		f_{LO} = 900MHz to 1300MHz, P_{LO} = +3dBm (Note 10)			-35	-23	dBm
RF-to-IF Isolation		f_{RF} = 824MHz to 915MHz (Note 10)		30	38		dB
LO-to-LO Isolation		P_{LO1} = +3dBm, P_{LO2} = +3dBm, f_{LO1} = 900MHz, f_{LO2} = 901MHz, P_{RF} = -5dBm (Notes 8, 10)		40	46		dB
Channel-to-Channel Isolation		RFMAIN (RFDIV) converted power measured at IFDIV (IFMAIN), relative to IFMAIN (IFDIV), all unused ports terminated to 50Ω (Note 9)		40	48		dB
LO Switching Time		50% of LOSEL to IF settled within 2 degrees			50	1000	ns
RF Input Impedance	Z_{RF}				50		Ω
RF Input Return Loss		LO on and IF terminated into matched impedance			20		dB
LO Input Impedance	Z_{LO}				50		Ω
LO Input Return Loss		RF and IF terminated into matched impedance, LO port selected			20		dB
		RF and IF terminated into matched impedance, LO port unselected			20		
IF Terminal Output Impedance	Z_{IF}	Nominal differential impedance at the IC's IF output			200		Ω
IF Return Loss		RF terminated in 50Ω; transformed to 50Ω using external components shown in the *Typical Application Circuit*			18		dB

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, RF and LO ports are driven from 50Ω sources. Typical values are at V_{CC} = +3.3V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 900MHz, f_{LO} = 1100MHz, f_{IF} = 200MHz, T_C =+25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Power Gain	G_C				8.7		dB
Conversion Power Gain Variation vs. Frequency	ΔG_C	Flatness over any one of three frequency bands: f_{RF} = 824MHz to 849MHz, f_{RF} = 869MHz to 894MHz, f_{RF} = 880MHz to 915MHz			0.15		dB
Gain Variation Over Temperature	TC_G	T_C = -40°C to +85°C			-0.012		dB/°C
Noise Figure	NF				9.0		dB
Noise Figure Temperature Coefficient	TC_{NF}	T_C = -40°C to +85°C			0.018		dB/°C
Input 1dB Compression Point	IP_{1dB}				10.6		dBm
Third-Order Input Intercept Point	IIP3	f_{RF1} = 900MHz, f_{RF2} = 901MHz, f_{IF} = 200MHz, P_{RF} = -5dBm/tone			24.7		dBm
2LO-2RF Spur Rejection	2 x 2	f_{RF} = 800MHz, f_{LO} = 1000MHz, f_{SPUR} = 900MHz	P_{RF} = -10dBm		-74.9		dBc
			P_{RF} = -5dBm		-69.9		
3LO-3RF Spur Rejection	3 x 3	f_{RF} = 800MHz, f_{LO} = 1000MHz, f_{SPUR} = 933.333MHz	P_{RF} = -10dBm		-78		dBc
			P_{RF} = -5dBm		-73		
Maximum LO Leakage at RF Port		f_{LO} = 900MHz to 1300MHz, P_{LO} = +3dBm			-40		dBm
Maximum 2LO Leakage at RF Port		f_{LO} = 900MHz to 1300MHz, P_{LO} = +3dBm			-42		dBm
Maximum LO Leakage at IF Port		f_{LO} = 900MHz to 1300MHz, P_{LO} = +3dBm			-34		dBm
Minimum RF-to-IF Isolation		f_{RF} = 824MHz to 915MHz			38		dB
LO-to-LO Isolation		P_{LO1} = +3dBm, P_{LO2} = +3dBm, f_{LO1} = 900MHz, f_{LO2} = 901MHz (Note 8)			45		dB
Channel-to-Channel Isolation		RFMAIN (RFDIV) converted power measured at IFDIV (IFMAIN), relative to IFMAIN (IFDIV), all unused ports terminated to 50Ω			48		dB
LO Switching Time		50% of LOSEL to IF settled within 2 degrees			50		ns
RF Input Impedance	Z_{RF}				50		Ω
RF Input Return Loss		LO on and IF terminated into matched impedance			21		dB
LO Input Impedance	Z_{LO}				50		Ω
LO Input Return Loss		RF and IF terminated into matched impedance, LO port selected			31		dB
		RF and IF terminated into matched impedance, LO port unselected			24		

Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, RF and LO ports are driven from 50Ω sources. Typical values are at V_{CC} = +3.3V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 900MHz, f_{LO} = 1100MHz, f_{IF} = 200MHz, T_C =+25°C, unless otherwise noted.) (Note 6)

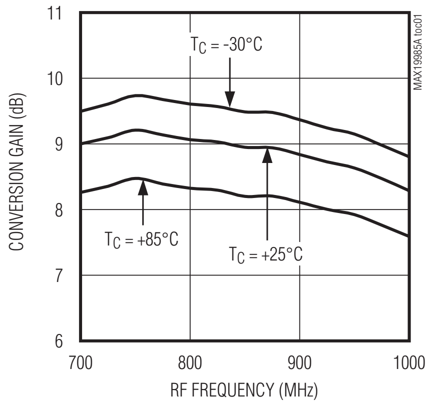
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IF Terminal Output Impedance	Z_{IF}	Nominal differential impedance at the IC's IF output		200		Ω
IF Output Return Loss		RF terminated in 50Ω; transformed to 50Ω using external components shown in the *Typical Application Circuit*		17		dB

Note 5: Not production tested. Operation outside this range is possible, but with degraded performance of some parameters. See the *Typical Operating Characteristics*. Performance is optimized for RF frequencies of 824MHz to 915MHz.
Note 6: All limits reflect losses of external components. Output measurements taken at IF outputs of *Typical Application Circuit*.
Note 7: Measured with external LO source noise filtered so the noise floor is -174dBm/Hz. This specification reflects the effects of all SNR degradations in the mixer including the LO noise, as defined in the Application Note 2021: *Specifications and Measurement of Local Oscillator Noise in Integrated Circuit Base Station Mixers*.
Note 8: Measured at IF port at IF frequency. LOSEL may be in any logic state.
Note 9: Limited production testing.
Note 10: Guaranteed by production testing.

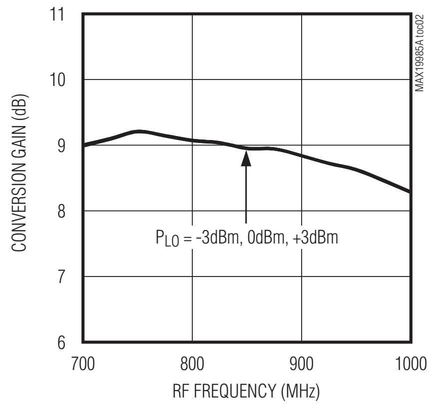
Typical Operating Characteristics

(*Typical Application Circuit*, $\mathbf{V_{CC} = +5.0V}$, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

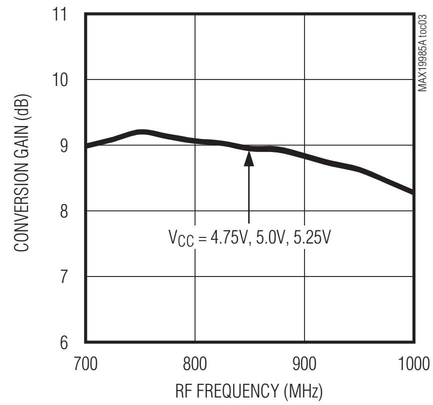
CONVERSION GAIN vs. RF FREQUENCY



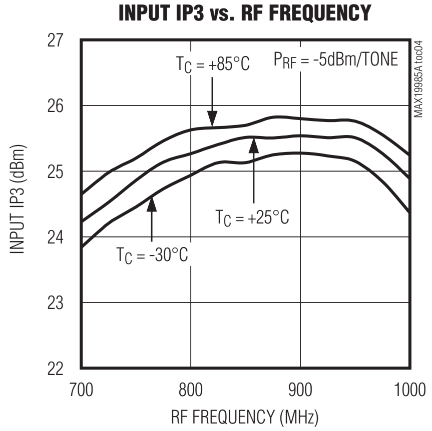
CONVERSION GAIN vs. RF FREQUENCY



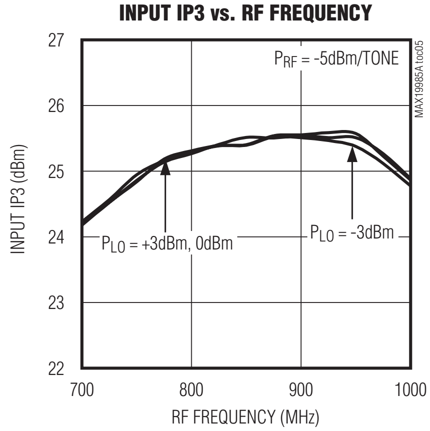
CONVERSION GAIN vs. RF FREQUENCY



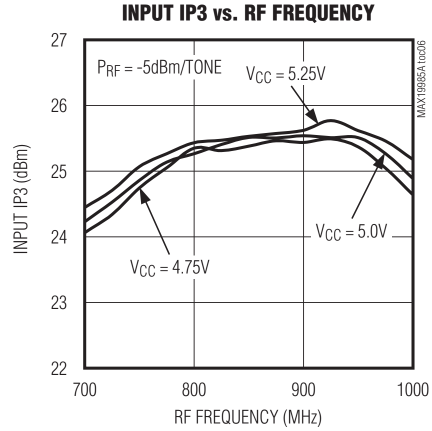
INPUT IP3 vs. RF FREQUENCY



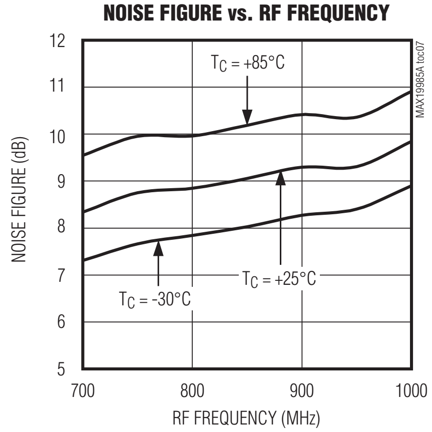
INPUT IP3 vs. RF FREQUENCY



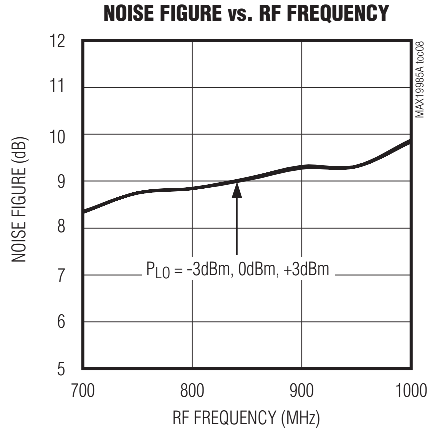
INPUT IP3 vs. RF FREQUENCY



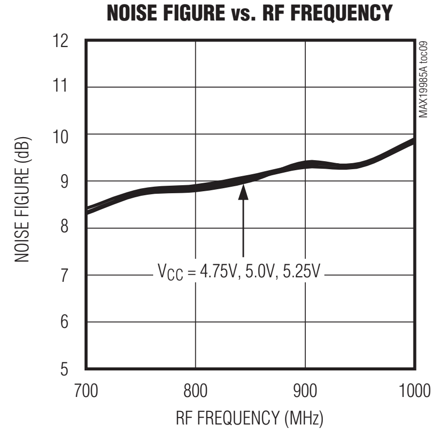
NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY



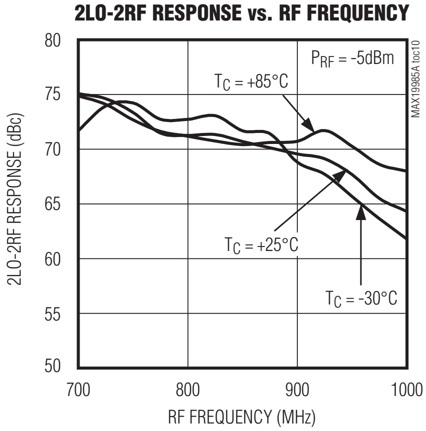
NOISE FIGURE vs. RF FREQUENCY



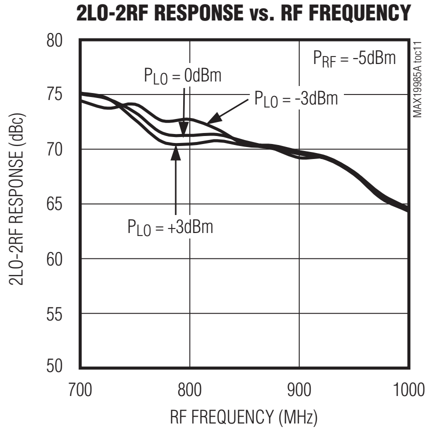
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +5.0V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

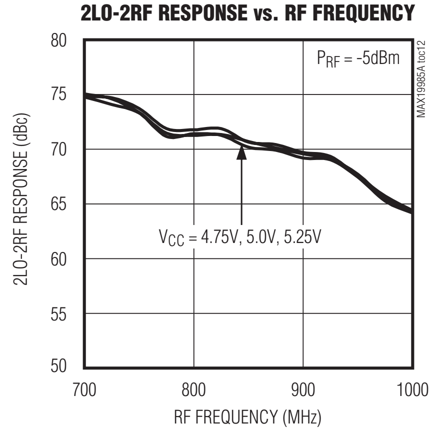
2LO-2RF RESPONSE vs. RF FREQUENCY



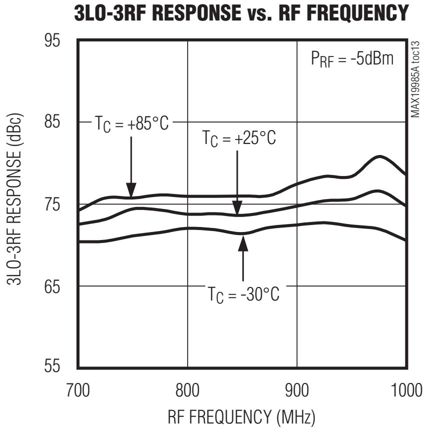
2LO-2RF RESPONSE vs. RF FREQUENCY



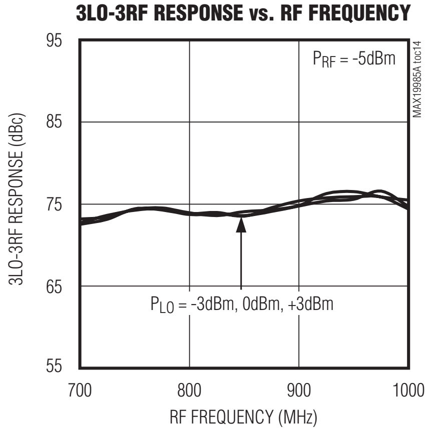
2LO-2RF RESPONSE vs. RF FREQUENCY



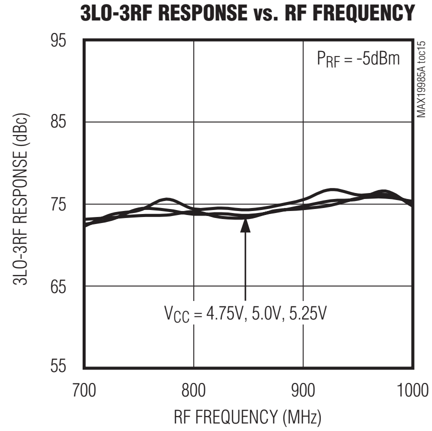
3LO-3RF RESPONSE vs. RF FREQUENCY



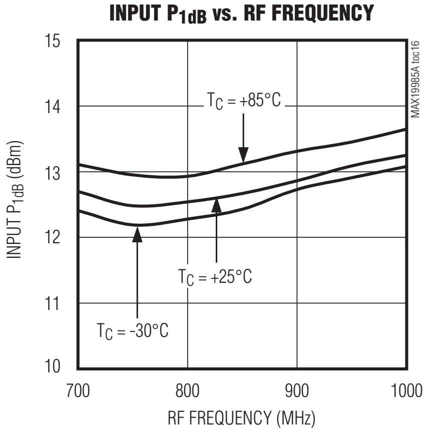
3LO-3RF RESPONSE vs. RF FREQUENCY



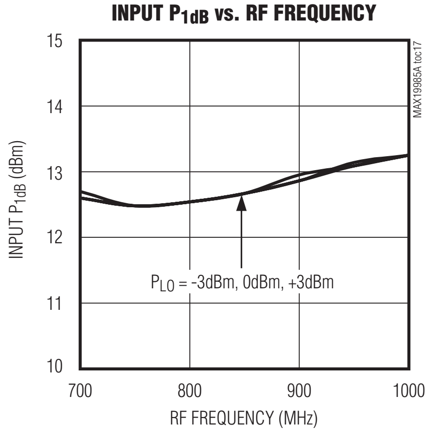
3LO-3RF RESPONSE vs. RF FREQUENCY



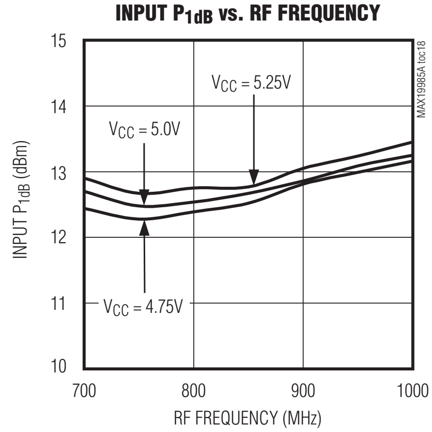
INPUT P_{1dB} vs. RF FREQUENCY



INPUT P_{1dB} vs. RF FREQUENCY



INPUT P_{1dB} vs. RF FREQUENCY

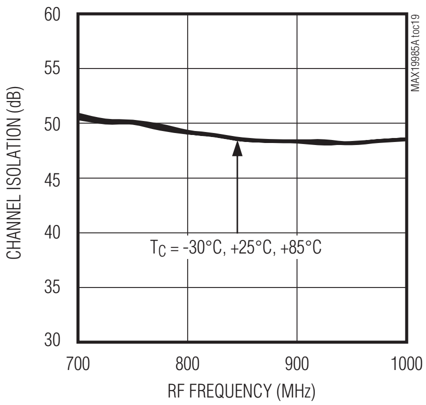


Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

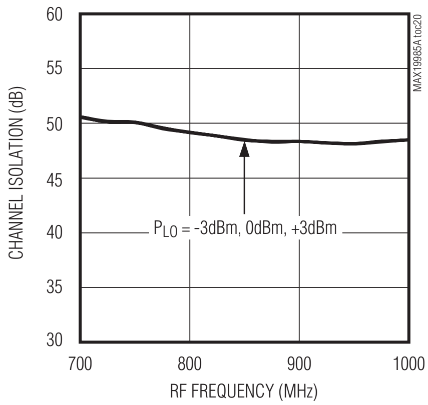
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +5.0V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

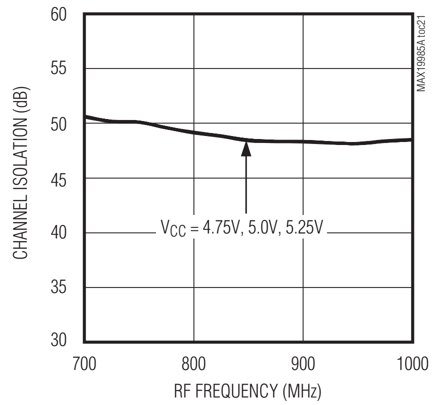
CHANNEL ISOLATION vs. RF FREQUENCY



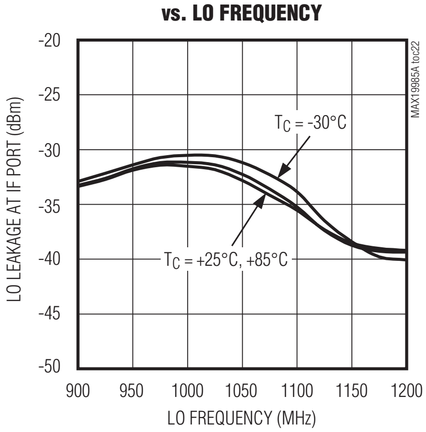
CHANNEL ISOLATION vs. RF FREQUENCY



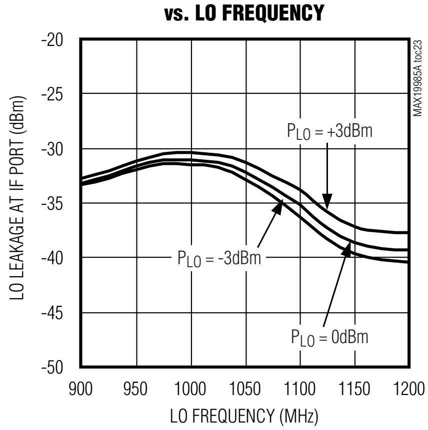
CHANNEL ISOLATION vs. RF FREQUENCY



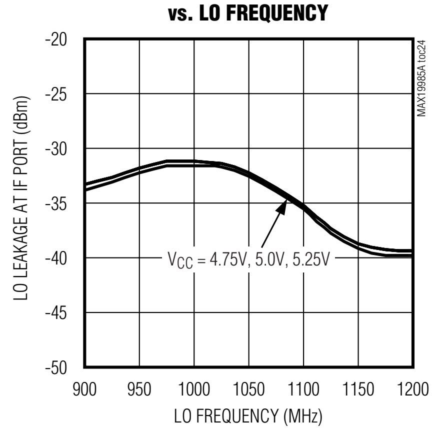
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



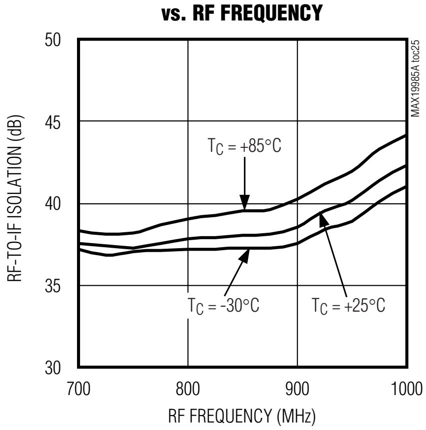
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



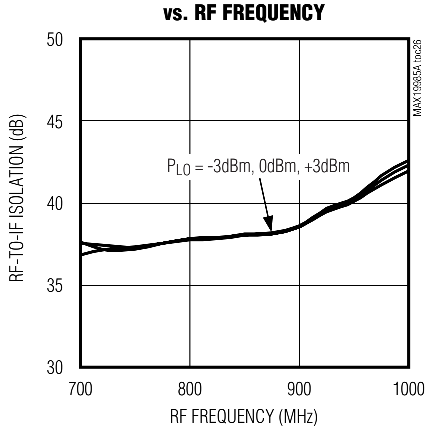
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



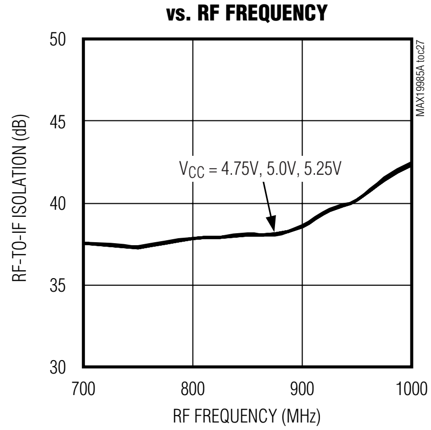
RF-TO-IF ISOLATION vs. RF FREQUENCY



RF-TO-IF ISOLATION vs. RF FREQUENCY



RF-TO-IF ISOLATION vs. RF FREQUENCY

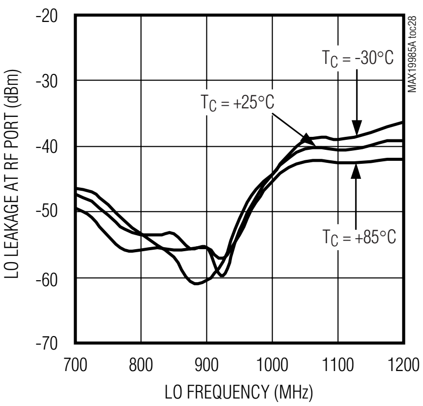


Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

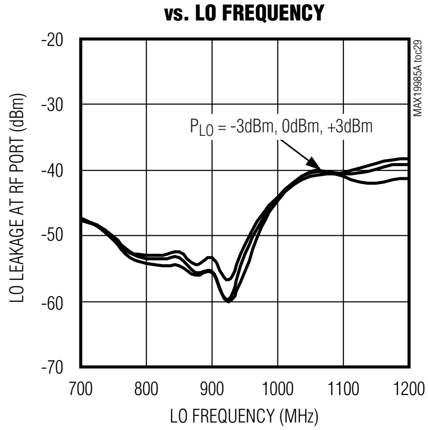
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +5.0V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

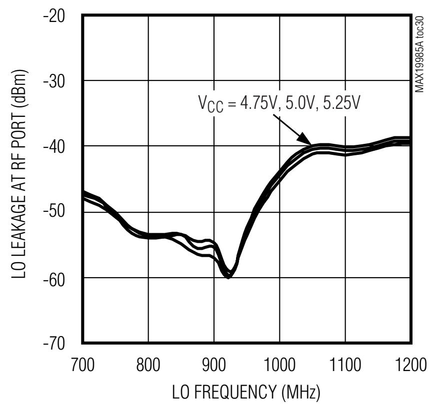
LO LEAKAGE AT RF PORT vs. LO FREQUENCY



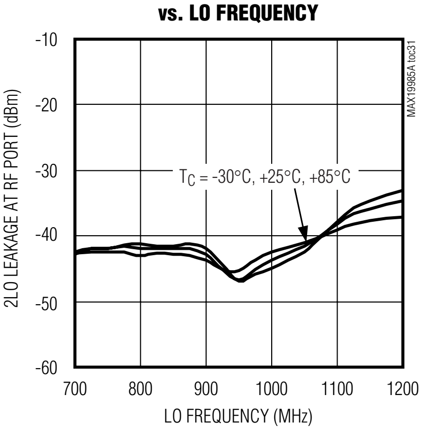
LO LEAKAGE AT RF PORT vs. LO FREQUENCY



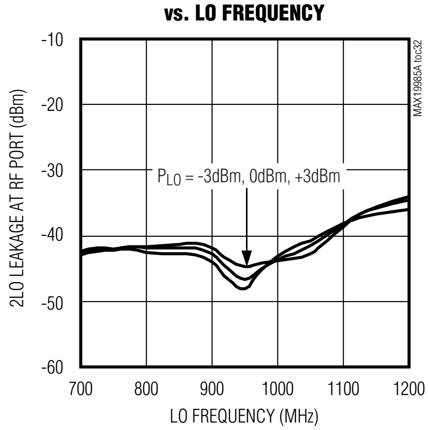
LO LEAKAGE AT RF PORT vs. LO FREQUENCY



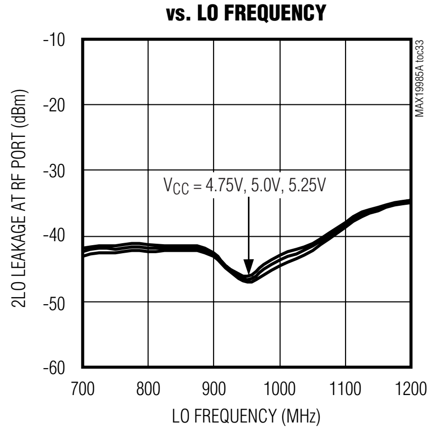
2LO LEAKAGE AT RF PORT vs. LO FREQUENCY



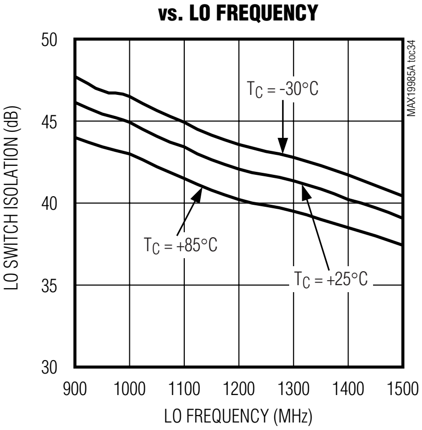
2LO LEAKAGE AT RF PORT vs. LO FREQUENCY



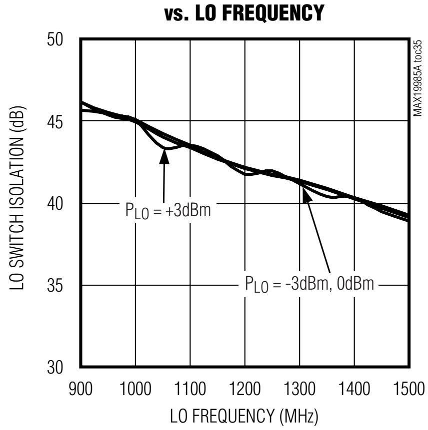
2LO LEAKAGE AT RF PORT vs. LO FREQUENCY



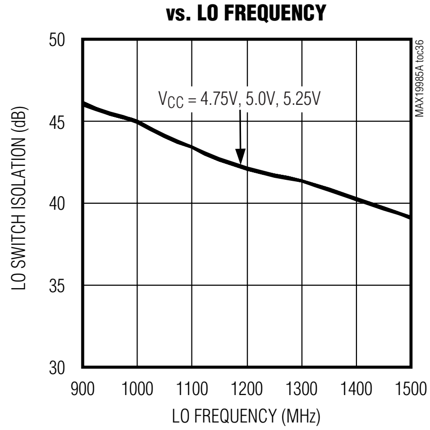
LO SWITCH ISOLATION vs. LO FREQUENCY



LO SWITCH ISOLATION vs. LO FREQUENCY



LO SWITCH ISOLATION vs. LO FREQUENCY

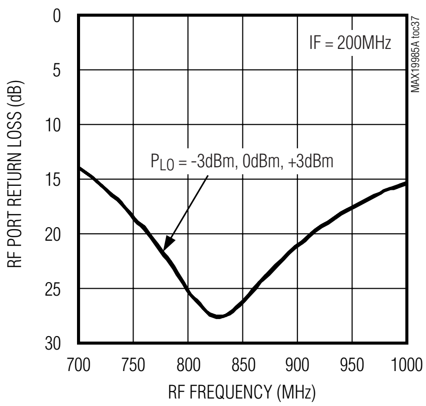


Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

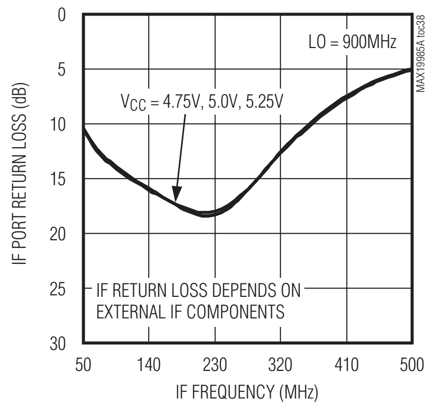
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +5.0V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

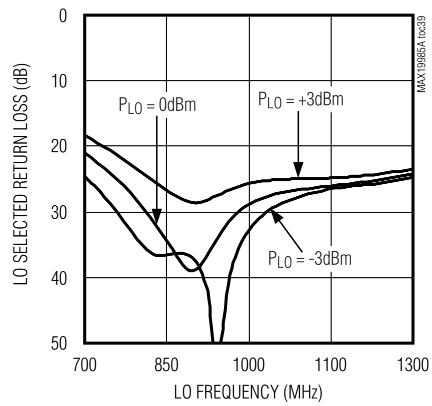
RF PORT RETURN LOSS vs. RF FREQUENCY



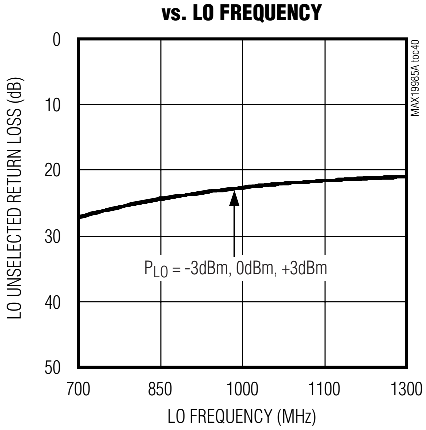
IF PORT RETURN LOSS vs. IF FREQUENCY



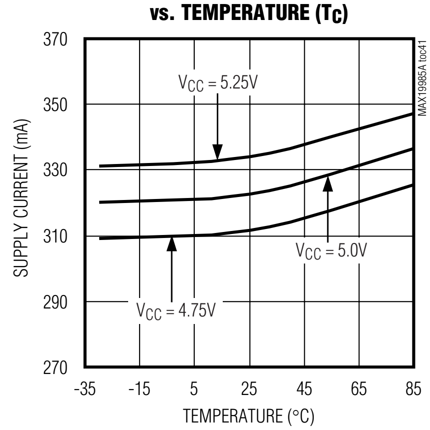
LO SELECTED RETURN LOSS vs. LO FREQUENCY



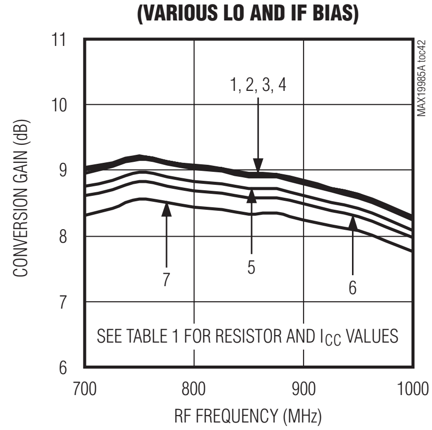
LO UNSELECTED RETURN LOSS vs. LO FREQUENCY



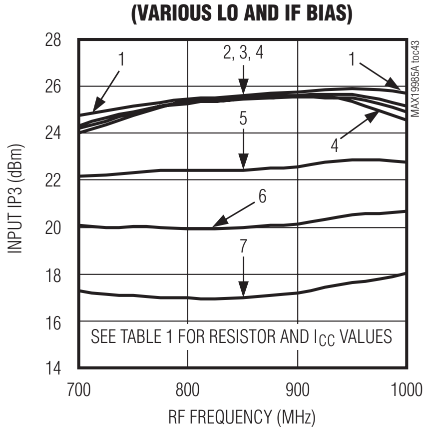
SUPPLY CURRENT vs. TEMPERATURE (T_C)



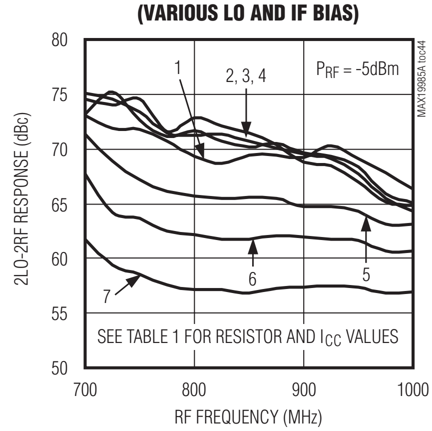
CONVERSION GAIN vs. RF FREQUENCY (VARIOUS LO AND IF BIAS)



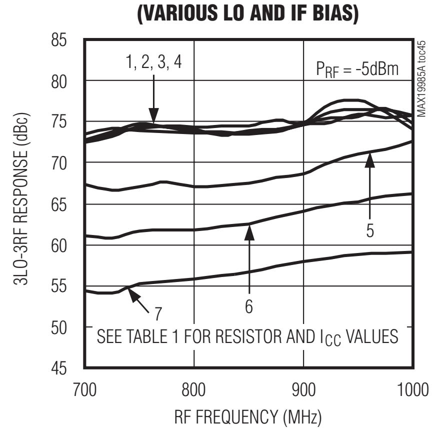
INPUT IP3 vs. RF FREQUENCY (VARIOUS LO AND IF BIAS)



2LO-2RF RESPONSE vs. RF FREQUENCY (VARIOUS LO AND IF BIAS)



3LO-3RF RESPONSE vs. RF FREQUENCY (VARIOUS LO AND IF BIAS)

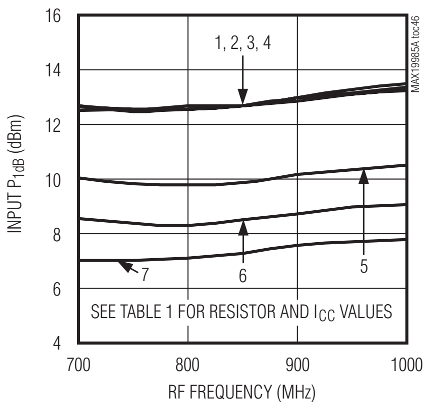


Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

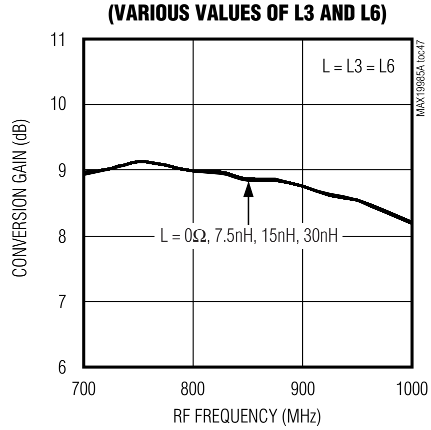
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +5.0V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

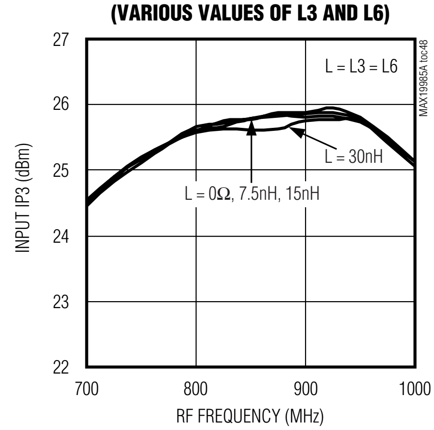
INPUT P_{1dB} vs. RF FREQUENCY (VARIOUS LO AND IF BIAS)



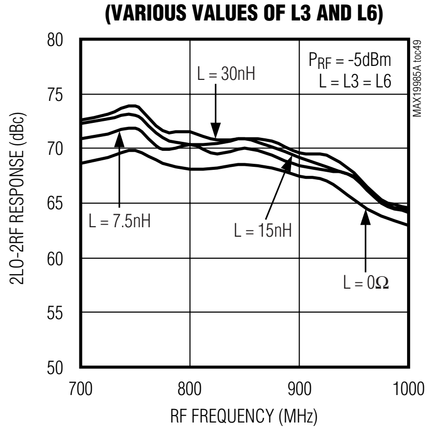
CONVERSION GAIN vs. RF FREQUENCY (VARIOUS VALUES OF L3 AND L6)



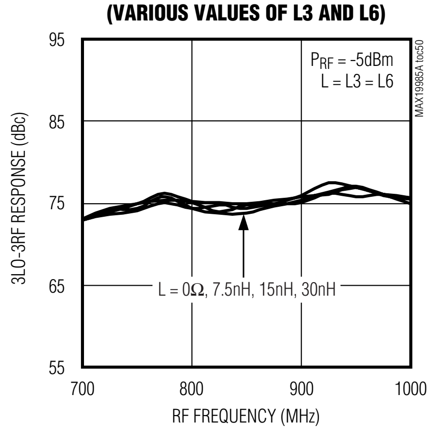
INPUT IP3 vs. RF FREQUENCY (VARIOUS VALUES OF L3 AND L6)



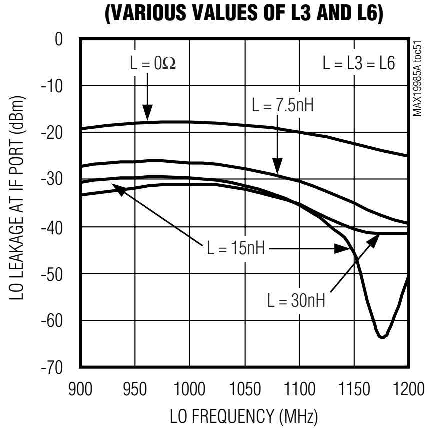
2LO-2RF RESPONSE vs. RF FREQUENCY (VARIOUS VALUES OF L3 AND L6)



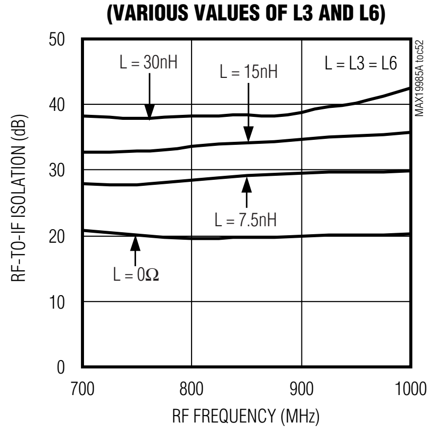
3LO-3RF RESPONSE vs. RF FREQUENCY (VARIOUS VALUES OF L3 AND L6)



LO LEAKAGE AT IF PORT vs. LO FREQUENCY (VARIOUS VALUES OF L3 AND L6)



RF-TO-IF ISOLATION vs. RF FREQUENCY (VARIOUS VALUES OF L3 AND L6)

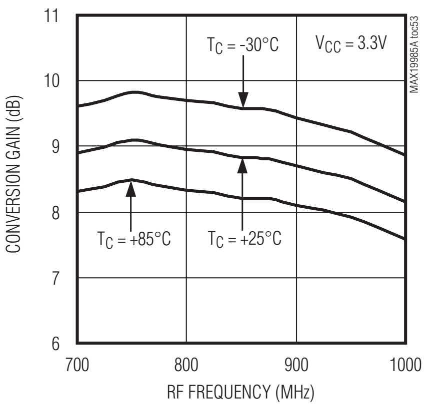


Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

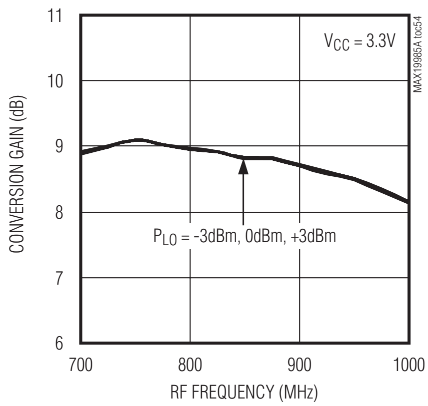
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +3.3V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

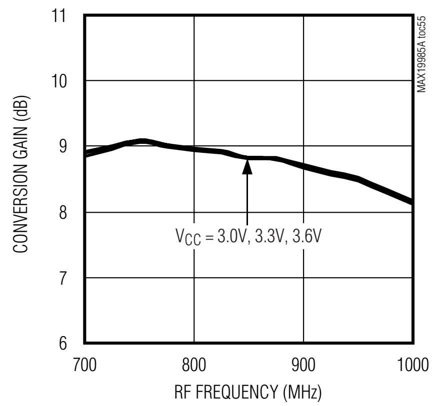
CONVERSION GAIN vs. RF FREQUENCY



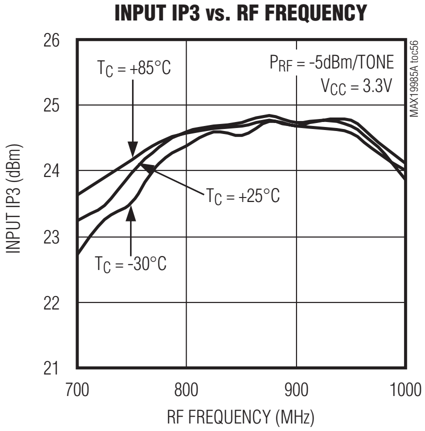
CONVERSION GAIN vs. RF FREQUENCY



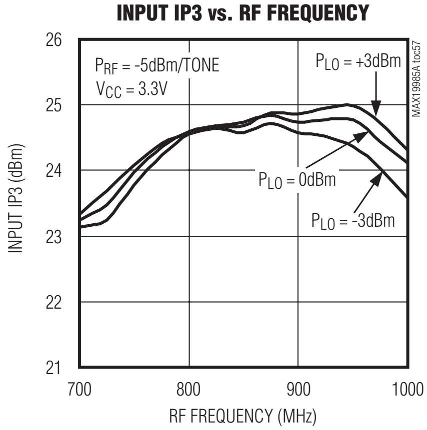
CONVERSION GAIN vs. RF FREQUENCY



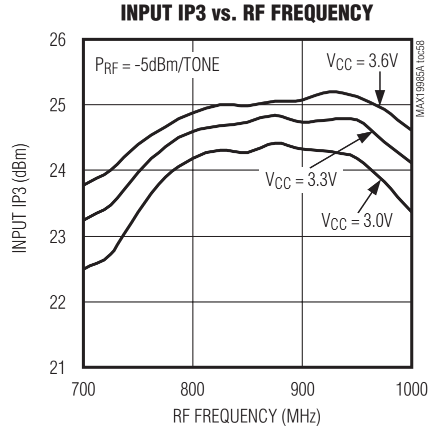
INPUT IP3 vs. RF FREQUENCY



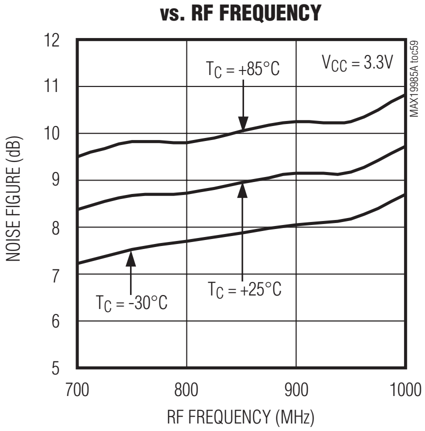
INPUT IP3 vs. RF FREQUENCY



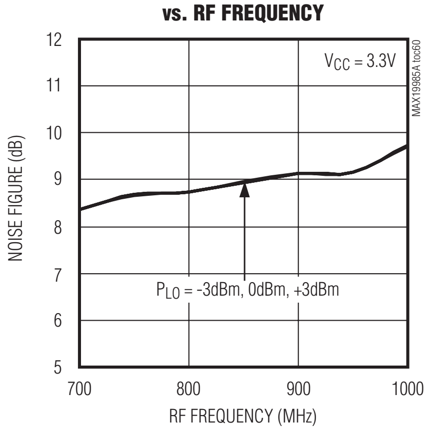
INPUT IP3 vs. RF FREQUENCY



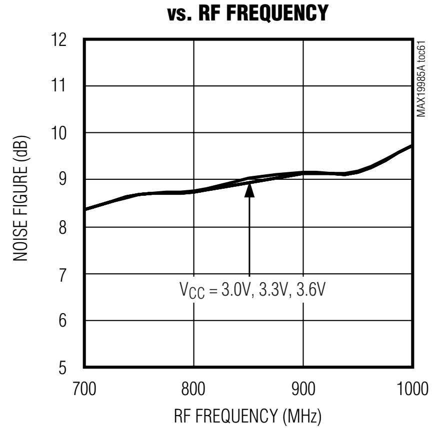
NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY

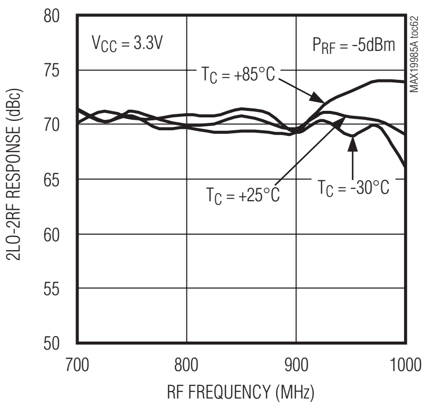


Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

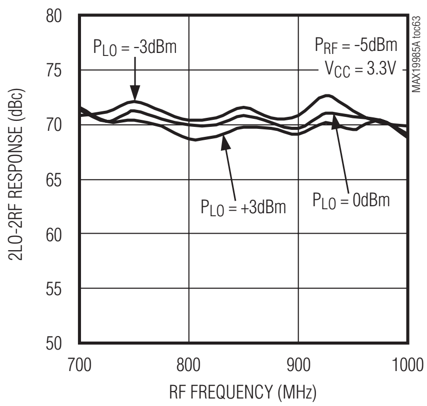
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +3.3V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

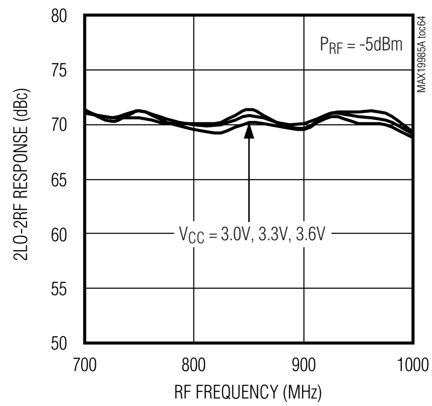
2LO-2RF RESPONSE vs. RF FREQUENCY



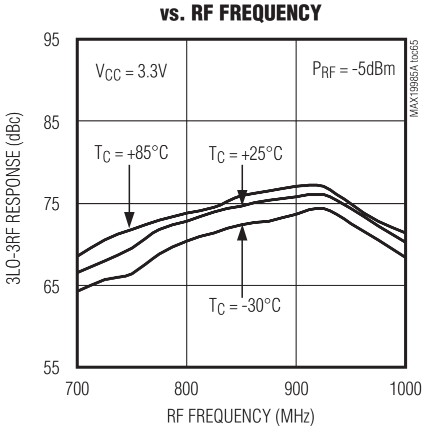
2LO-2RF RESPONSE vs. RF FREQUENCY



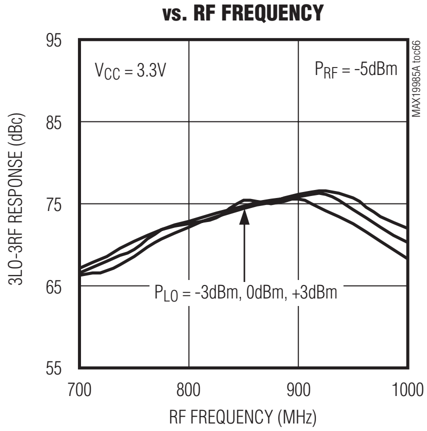
2LO-2RF RESPONSE vs. RF FREQUENCY



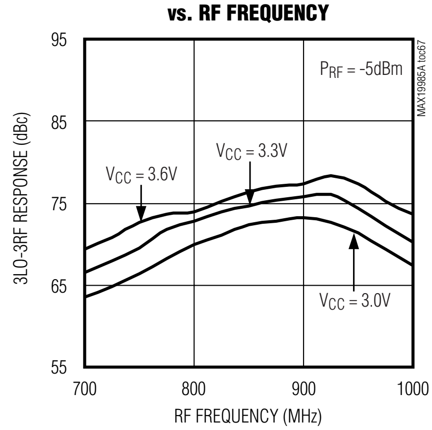
3LO-3RF RESPONSE vs. RF FREQUENCY



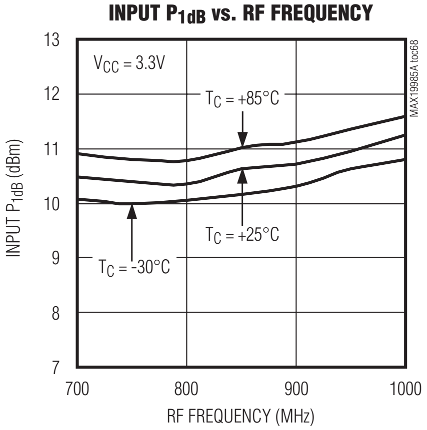
3LO-3RF RESPONSE vs. RF FREQUENCY



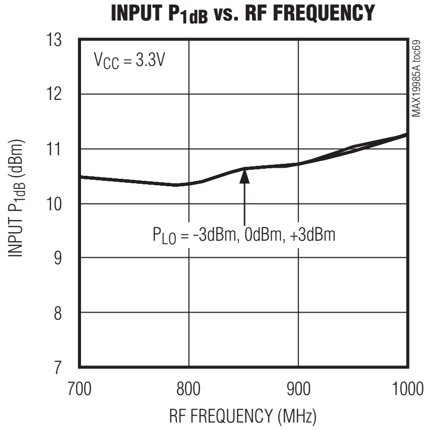
3LO-3RF RESPONSE vs. RF FREQUENCY



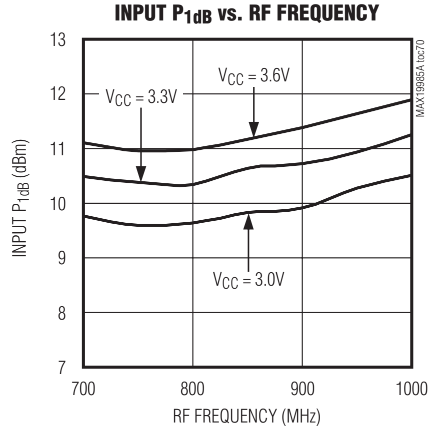
INPUT P_{1dB} vs. RF FREQUENCY



INPUT P_{1dB} vs. RF FREQUENCY



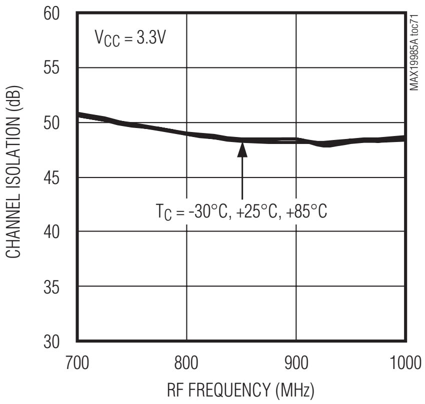
INPUT P_{1dB} vs. RF FREQUENCY



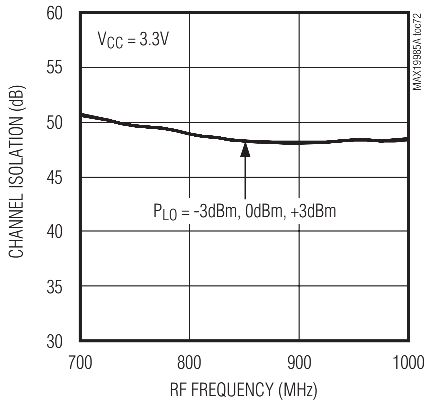
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +3.3V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

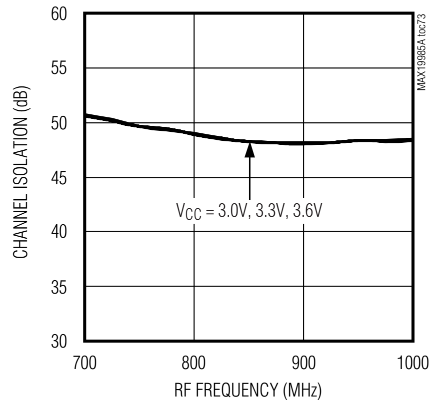
CHANNEL ISOLATION vs. RF FREQUENCY



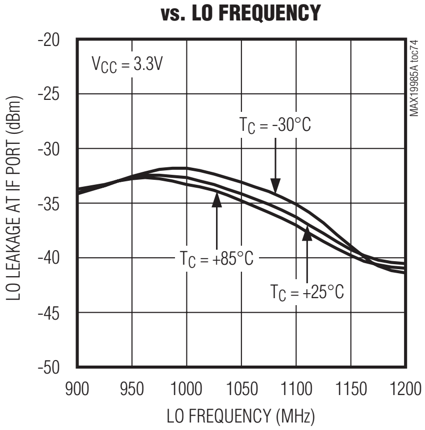
CHANNEL ISOLATION vs. RF FREQUENCY



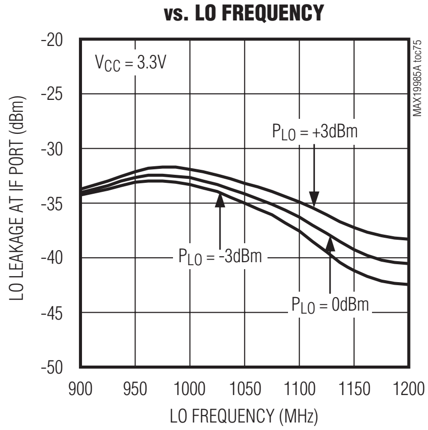
CHANNEL ISOLATION vs. RF FREQUENCY



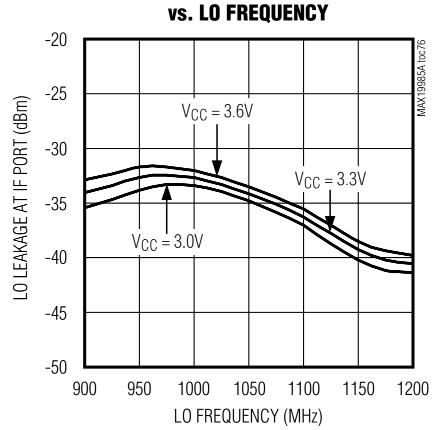
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



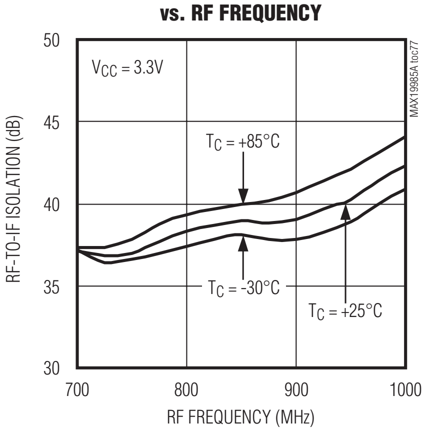
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



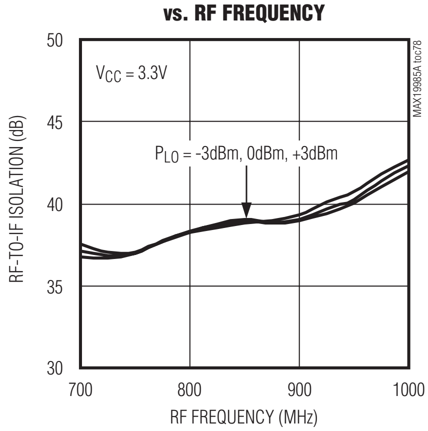
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



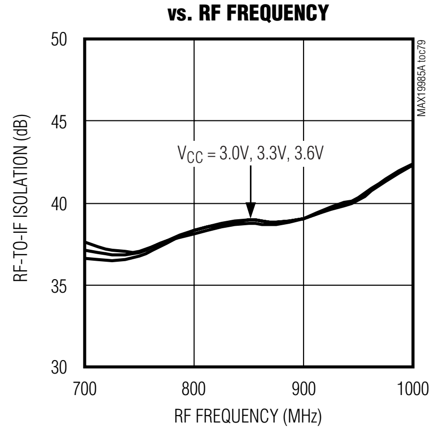
RF-TO-IF ISOLATION vs. RF FREQUENCY



RF-TO-IF ISOLATION vs. RF FREQUENCY



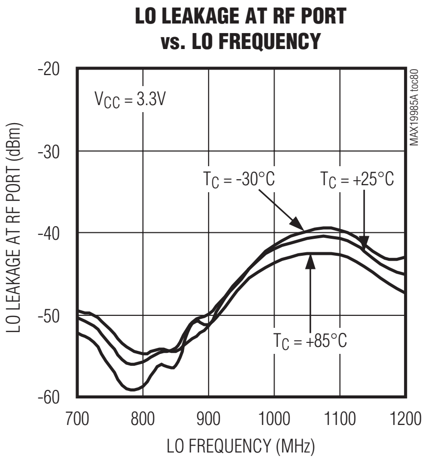
RF-TO-IF ISOLATION vs. RF FREQUENCY

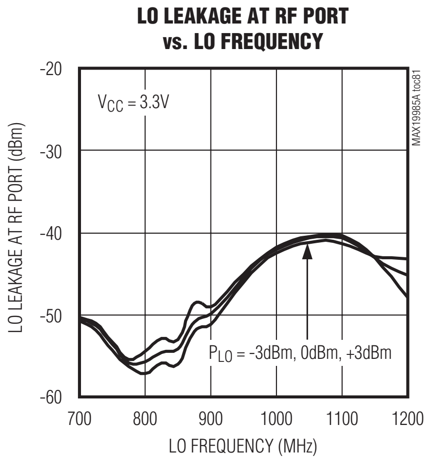


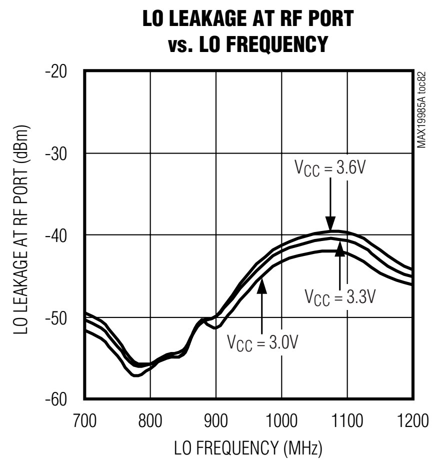
Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

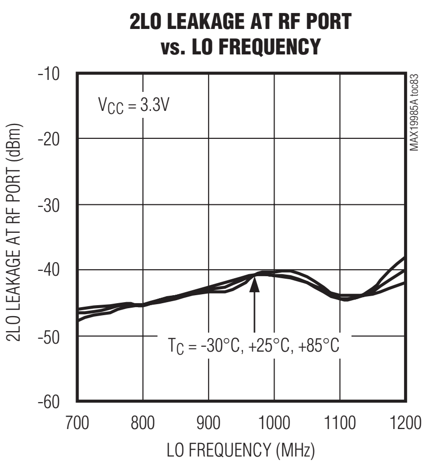
Typical Operating Characteristics (continued)

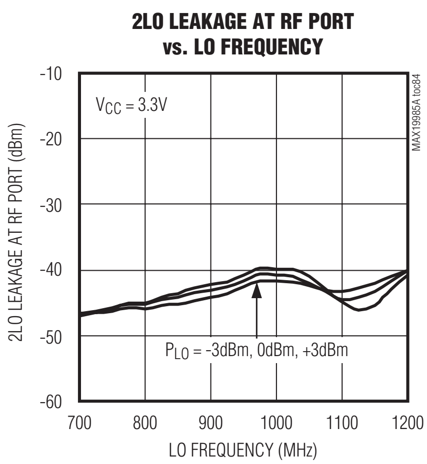
(*Typical Application Circuit*, **V_{CC} = +3.3V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

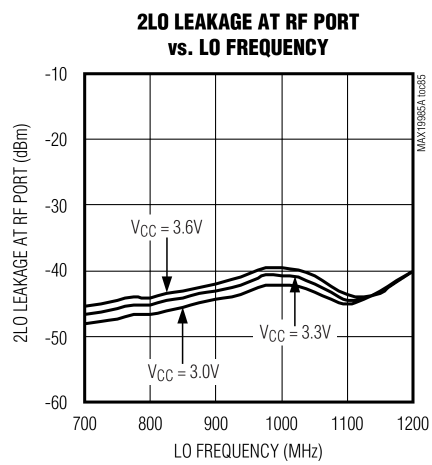


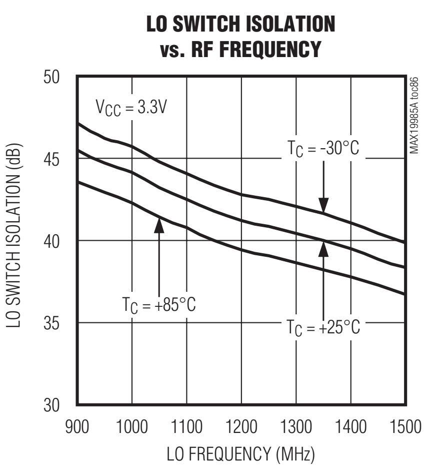


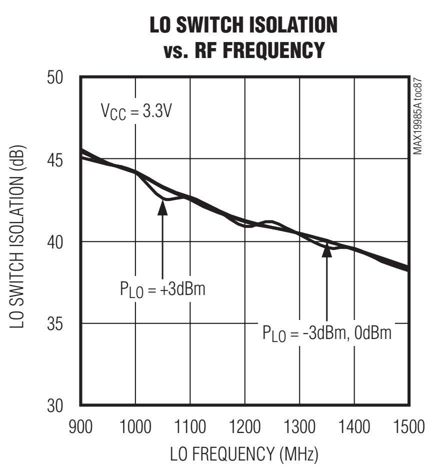


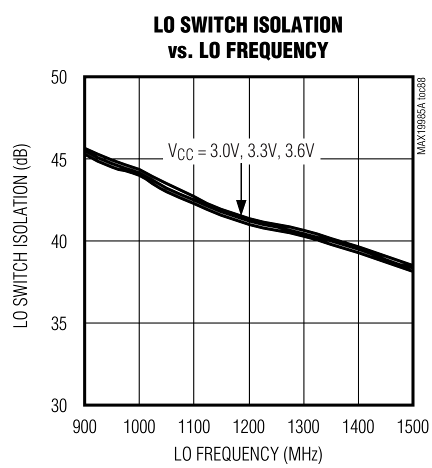








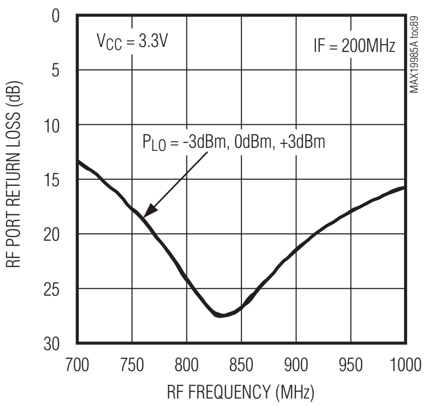




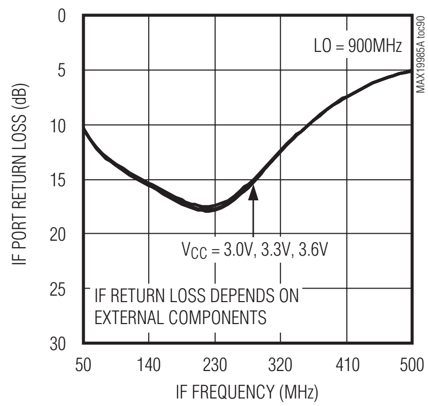
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = +3.3V**, P_{LO} = 0dBm, P_{RF} = -5dBm, LO is high-side injected for a 200MHz IF, T_C =+25°C, unless otherwise noted.)

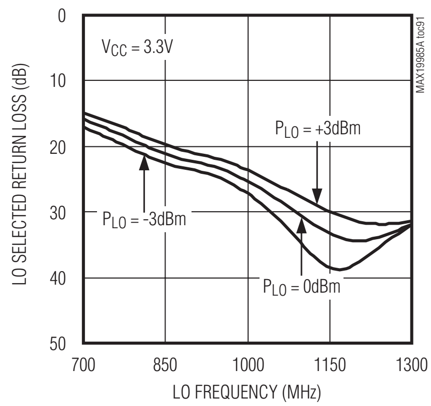
RF PORT RETURN LOSS vs. RF FREQUENCY



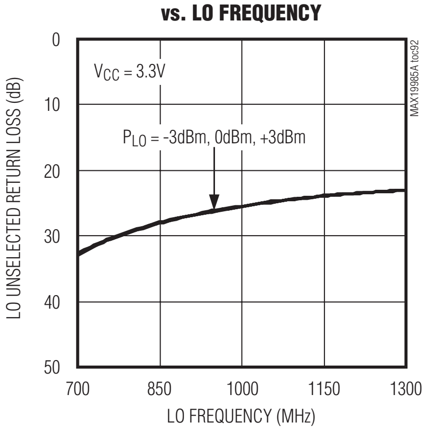
IF PORT RETURN LOSS vs. IF FREQUENCY



LO SELECTED RETURN LOSS vs. LO FREQUENCY



LO UNSELECTED RETURN LOSS vs. LO FREQUENCY



SUPPLY CURRENT vs. TEMPERATURE (T_C)

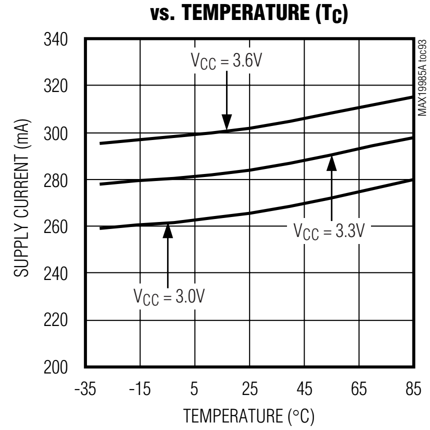


Table 1. DC Current vs. Bias Resistor Settings

BIAS CONDITION	DC CURRENT (mA)	R1 AND R4 VALUES (Ω)	R2 AND R5 VALUES (Ω)
1	359.4	698	800
2	331.8	698	1100
3	322.8	698	1200
4	311.7	698	1400
5	268.2	1100	1200
6	244.4	1400	1200
7	223.7	1820	1200

Note: *See TOCs 42–46 for performance trade-offs vs. DC bias condition.*

Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

Pin Description

PIN	NAME	FUNCTION
1	RFMAIN	Main Channel RF input. Internally matched to 50Ω. Requires an input DC-blocking capacitor.
2	TAPMAIN	Main Channel Balun Center Tap. Bypass to GND with 39pF and 0.033µF capacitors as close as possible to the pin with the smaller value capacitor closer to the part.
3, 5, 7, 12, 20, 22, 24, 25, 26, 34	GND	Ground
4, 6, 10, 16, 21, 30, 36	V_{CC}	Power Supply. Bypass to GND with 0.01µF capacitors as close as possible to the pin. Pins 4 and 6 do not require bypass capacitors.
8	TAPDIV	Diversity Channel Balun Center Tap. Bypass to GND with 39pF and 0.033µF capacitors as close as possible to the pin with the smaller value capacitor closer to the part.
9	RFDIV	Diversity Channel RF Input. Internally matched to 50Ω. Requires an input DC-blocking capacitor.
11	IFDBIAS	IF Diversity Amplifier Bias Control. Connect a resistor from this pin to ground to set the bias current for the diversity IF amplifier (see the *Typical Operating Characteristics* for typical performance vs. resistor value).
13, 14	IFD+, IFD-	Diversity Mixer Differential IF Outputs. Connect pullup inductors from each of these pins to V_{CC} (see the *Typical Application Circuit*).
15	LEXTD	Diversity External Inductor Connection. Connect a parallel combination of an inductor and a 500Ω resistor from this pin to ground to increase the RF-to-IF and LO-to-IF isolation (see the *Typical Operating Characteristics* for typical performance vs. inductor value).
17	LODBIAS	LO Diversity Amplifier Bias Control. Connect a resistor from this pin to ground to set the bias current for the diversity LO amplifier (see the *Typical Operating Characteristics* for typical performance vs. resistor value).
18, 28	N.C.	No Connection. Not internally connected.
19	LO1	Local Oscillator 1 Input. This input is internally matched to 50Ω. Requires an input DC-blocking capacitor.
23	LOSEL	Local Oscillator Select. Set this pin to high to select LO1. Set to low to select LO2.
27	LO2	Local Oscillator 2 Input. This input is internally matched to 50Ω. Requires an input DC-blocking capacitor.
29	LOMBIAS	LO Main Amplifier Bias Control. Connect a resistor from this pin to ground to set the bias current for the main LO amplifier (see the *Typical Operating Characteristics* for typical performance vs. resistor value).
31	LEXTM	Main External Inductor Connection. Connect a parallel combination of an inductor and a 500Ω resistor from this pin to ground to increase the RF-to-IF and LO-to-IF isolation (see *Typical Operating Characteristics* for typical performance vs. inductor value).
32, 33	IFM-, IFM+	Main Mixer Differential IF Outputs. Connect pullup inductors from each of these pins to V_{CC} (see the *Typical Application Circuit*).
35	IFMBIAS	IF Main Amplifier Bias Control. Connect a resistor from this pin to ground to set the bias current for the main IF amplifier (see the *Typical Operating Characteristics* for typical performance vs. resistor value).
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane using multiple vias to maximize thermal and RF performance.

Detailed Description

The MAX19985A is a dual-channel downconverter designed to provide 8.7dB of conversion gain, +25.5dBm of IIP3, +12.6dBm typical input 1dB compression point, and a 9.0dB noise figure.

In addition to its high-linearity performance, the MAX19985A achieves a high level of component integration. The device integrates two double-balanced mixers for two-channel downconversion. Both the main and diversity channels include a balun and matching circuitry to allow 50Ω single-ended interfaces to the RF ports and the two LO ports. An integrated single-pole/double-throw (SPDT) switch provides 50ns switching time between the two LO inputs with 46dB of LO-to-LO isolation and -40dBm of LO leakage at the RF port. Furthermore, the integrated LO buffers provide a high drive level to each mixer core, reducing the LO drive required at the MAX19985A's inputs to a range of -3dBm to +3dBm. The IF ports for both channels incorporate differential outputs for downconversion, which is ideal for providing enhanced 2LO-2RF performance.

Specifications are guaranteed over broad frequency ranges to allow for use in WCDMA, GSM/EDGE, iDEN, cdma2000, and LTE/WiMAX cellular and 700MHz band base stations. The MAX19985A is specified to operate over an RF input range of 700MHz to 1000MHz, an LO range of 900MHz to 1300MHz, and an IF range of 50MHz to 500MHz. The external IF components set the lower frequency range (see the *Typical Operating Characteristics* for details). Operation beyond these ranges is possible (see the *Typical Operating Characteristics* for additional information). Although this device is optimized for high-side LO injection applications, it can operate in low-side LO injection modes as well. However, performance degrades as f_{LO} continues to decrease. For increased low-side LO performance, refer to the MAX19985 data sheet.

RF Port and Balun

The RF input ports of both the main and diversity channels are internally matched to 50Ω, requiring no external matching components. A DC-blocking capacitor is required as the input is internally DC shorted to ground through the on-chip balun. The RF port input return loss is typically 20dB over the RF frequency range of 770MHz to 915MHz.

LO Inputs, Buffer, and Balun

The MAX19985A is optimized for a 900MHz to 1300MHz LO frequency range. As an added feature, the MAX19985A includes an internal LO SPDT switch for use in frequency-hopping applications. The switch selects one of the two single-ended LO ports, allowing the external oscillator to settle on a particular frequency before it is switched in. LO switching time is typically 50ns, which is more than adequate for typical GSM applications. If frequency hopping is not employed, simply set the switch to either of the LO inputs. The switch is controlled by a digital input (LOSEL), where logic-high selects LO1 and logic-low selects LO2. LO1 and LO2 inputs are internally matched to 50Ω, requiring only an 82pF DC-blocking capacitor. To avoid damage to the part, voltage **MUST** be applied to V_{CC} before digital logic is applied to LOSEL. Alternatively, a 1kΩ resistor can be placed in series at the LOSEL to limit the input current in applications where LOSEL is applied before V_{CC}.

The main and diversity channels incorporate a two-stage LO buffer that allows for a wide-input power range for the LO drive. The on-chip low-loss baluns, along with LO buffers, drive the double-balanced mixers. All interfacing and matching components from the LO inputs to the IF outputs are integrated on-chip.

High-Linearity Mixer

The core of the MAX19985A dual-channel downconverter consists of two double-balanced, high-performance passive mixers. Exceptional linearity is provided by the large LO swing from the on-chip LO buffers. When combined with the integrated IF amplifiers, the cascaded IIP3, 2LO-2RF rejection, and noise figure performance are typically +25.5dBm, 76dBc, and 9.0dB, respectively.

Differential IF

The MAX19985A has an IF frequency range of 50MHz to 500MHz, where the low-end frequency depends on the frequency response of the external IF components. Note that these differential ports are ideal for providing enhanced IIP2 performance. Single-ended IF applications require a 4:1 (impedance ratio) balun to transform the 200Ω differential IF impedance to a 50Ω single-ended system. After the balun, the return loss is typically 18dB. The user can use a differential IF amplifier on the mixer IF ports, but a DC block is required on both IFD+/IFD- and IFM+/IFM- ports to keep external DC from entering the IF ports of the mixer.

Dual, SiGe, High-Linearity, 700MHz to 1000MHz Downconversion Mixer with LO Buffer/Switch

Applications Information

Input and Output Matching

The RF and LO inputs are internally matched to 50Ω. No matching components are required. The RF port input return loss is typically 20dB over the RF frequency range of 770MHz to 915MHz and return loss at the LO ports are typically 20dB over the entire LO range. RF and LO inputs require only DC-blocking capacitors for interfacing.

The IF output impedance is 200Ω (differential). For evaluation, an external low-loss 4:1 (impedance ratio) balun transforms this impedance to a 50Ω single-ended output (see the *Typical Application Circuit*).

Externally Adjustable Bias

Each channel of the MAX19985A has two pins (LO_BIAS, IF_BIAS) that allow external resistors to set the internal bias currents. Nominal values for these resistors are given in Table 2. Larger-value resistors can be used to reduce power dissipation at the expense of some performance loss. See the *Typical Operating Characteristics* to evaluate the power vs. performance tradeoff. If ±1% resistors are not readily available, ±5% resistors can be substituted.

LEXT_ Inductors

For applications requiring optimum RF-to-IF and LO-to-IF isolation, connect a parallel combination of a low-ESR inductor and a 500Ω resistor from LEXT_ (pins 15 and 31) to ground. When improved isolation is not required, connect LEXT_ to ground using a 0Ω resistance. See the *Typical Operating Characteristics* to evaluate the isolation vs. inductor value tradeoff.

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. The load impedance presented to the mixer must be so that any capacitance from both IF- and IF+ to ground does not exceed several picofarads. For the best performance, route the ground pin traces directly to the exposed pad under the package. The PCB exposed pad **MUST** be connected to the ground plane of the PCB. It is suggested that multiple vias be used to connect this pad to the lower-level ground planes. This method provides a good RF/thermal-conduction path for the device. Solder the exposed pad on the bottom of the

Table 2. Component Values

COMPONENT	VALUE	DESCRIPTION
C1, C2, C7, C8	39pF	Microwave capacitors (0402)
C3, C6	0.033µF	Microwave capacitors (0603)
C4, C5	—	Not used
C9, C13, C15, C17, C18	0.01µF	Microwave capacitors (0402)
C10, C11, C12, C19, C20, C21	150pF	Microwave capacitors (0603)
C14, C16	82pF	Microwave capacitors (0402)
L1, L2, L4, L5	330nH	Wire-wound high-Q inductors (0805)
L3, L6	30nH	Wire-wound high-Q inductors (0603). Smaller values can be used at the expense of some performance loss (see the *Typical Operating Characteristics*).
R1, R4	698Ω	±1% resistors (0402). Larger values can be used to reduce power at the expense of some performance loss (see the *Typical Operating Characteristics*).
R2, R5	1.2kΩ	±1% resistors (0402). Use for **V_{CC} = +5.0V** applications. Larger values can be used to reduce power at the expense of some performance loss (see the *Typical Operating Characteristics*).
	600Ω	±1% resistors (0402). Use for **V_{CC} = +3.3V** applications.
R3, R6	0Ω	±1% resistors (1206)
R7, R8	500Ω	±1% resistors (0402)
T1, T2	4:1	Transformers (200:50) Mini-Circuits TC4-1W-7A
U1	—	MAX19985A IC

device package to the PCB. The MAX19985A evaluation kit can be used as a reference for board layout. Gerber files are available upon request at **www.maxim-ic.com**.

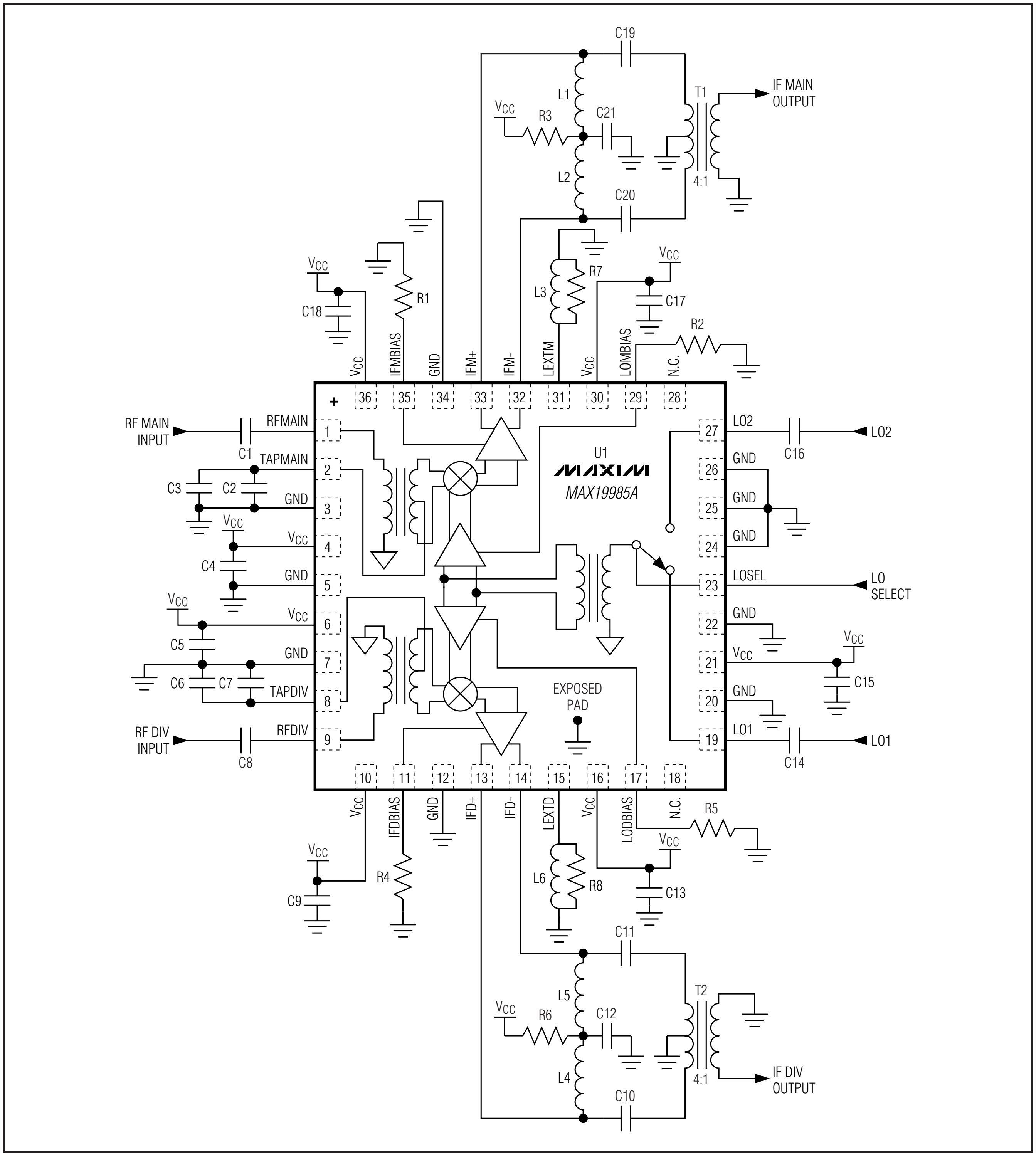
Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass each V_{CC} pin and TAPMAIN/TAPDIV with the capacitors shown in the *Typical Application Circuit* (see Table 2 for component values). Place the TAPMAIN/TAPDIV bypass capacitors to ground within 100 mils of the pin.

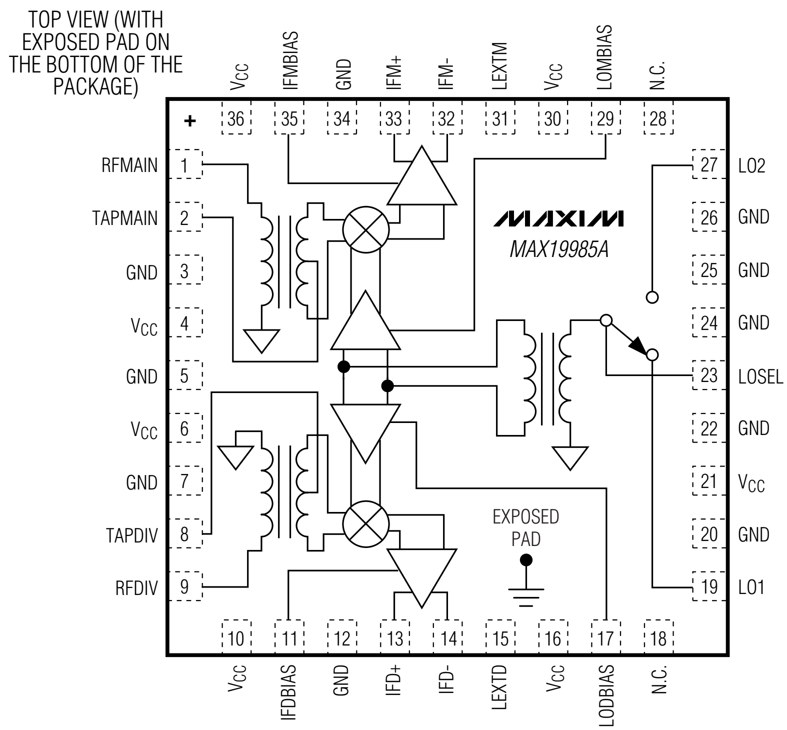
Exposed Pad RF/Thermal Considerations

The exposed pad (EP) of the MAX19985A's 36-pin thin QFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the MAX19985A is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Typical Application Circuit



Pin Configuration/Functional Diagram



THIN QFN-EP
6mm x 6mm

Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
36 Thin QFN-EP	T3666+2	21-0141